

FIG. 1

Phase	Vendor	Estimated Time (Days)
Order Processing	ASIC Provider	3
GD\$II Preparation	ASIC Provider	19
Fabrication	Fab	61
Probe Card Making	Test/Assembly House	56
Package Design	Test/Assembly House	56
Wafer Transfer	Freight Forwarder	1
Packaging	Test/Assembly House	3
Parts Transfer	Freight Forwarder	1
Test & Debug	ASIC Provider	5
Parts Transfer	Freight Forwarder	1
TOTAL		94

FIG. 2A

Phase	Vendor	Estimated Time(Days)
Order Processing	Fabless ASIC Provider	5
Fabrication	Foundry	68
Wafer Transfer	Freight Forwarder	1
Package/Test	Test/Assembly House	15
Parts Transfer	Freight Forwarder	1
TOTAL		90

FIG. 2B

Step No.	Step Name	Step Group
1	WAF-1	Wafer Start
9	TRCH1-CMP	Wafer Start
11	SAC1-OX	Wafer Start
25	PO1-DP	Gate Mask
27	PO1-ET	Gate Mask
63	ME1-PH	Metal 1
64	ME1-ET	Metal 1
76	VA2-CMP	Metal 3
76	VA2-CMP	Metal 3
117	PA1-PH	Metal 6
120	WAT 2-1	WAT
121	SORT	SORT

FIG. 2C

Title: Prediction Based Optimization of a Semiconductor Supply Chain
Using an Adaptive Real Time Work-in-Progress Tracking System
Applicants: Michael E. Orshansky and Klaus ten Hagen
Docket No.: 22272-06093

	Customer Order 1	Customer Order 2
Time Stamp	12:20 am, 06/20/01	12:20 am, 06/20/01
Foundry ID	5910	5920
Lot ID	5910-1	5920-2
Current Step	WAF1-START	WAF1-START
Current Quantity	25	25
....

FIG. 2D

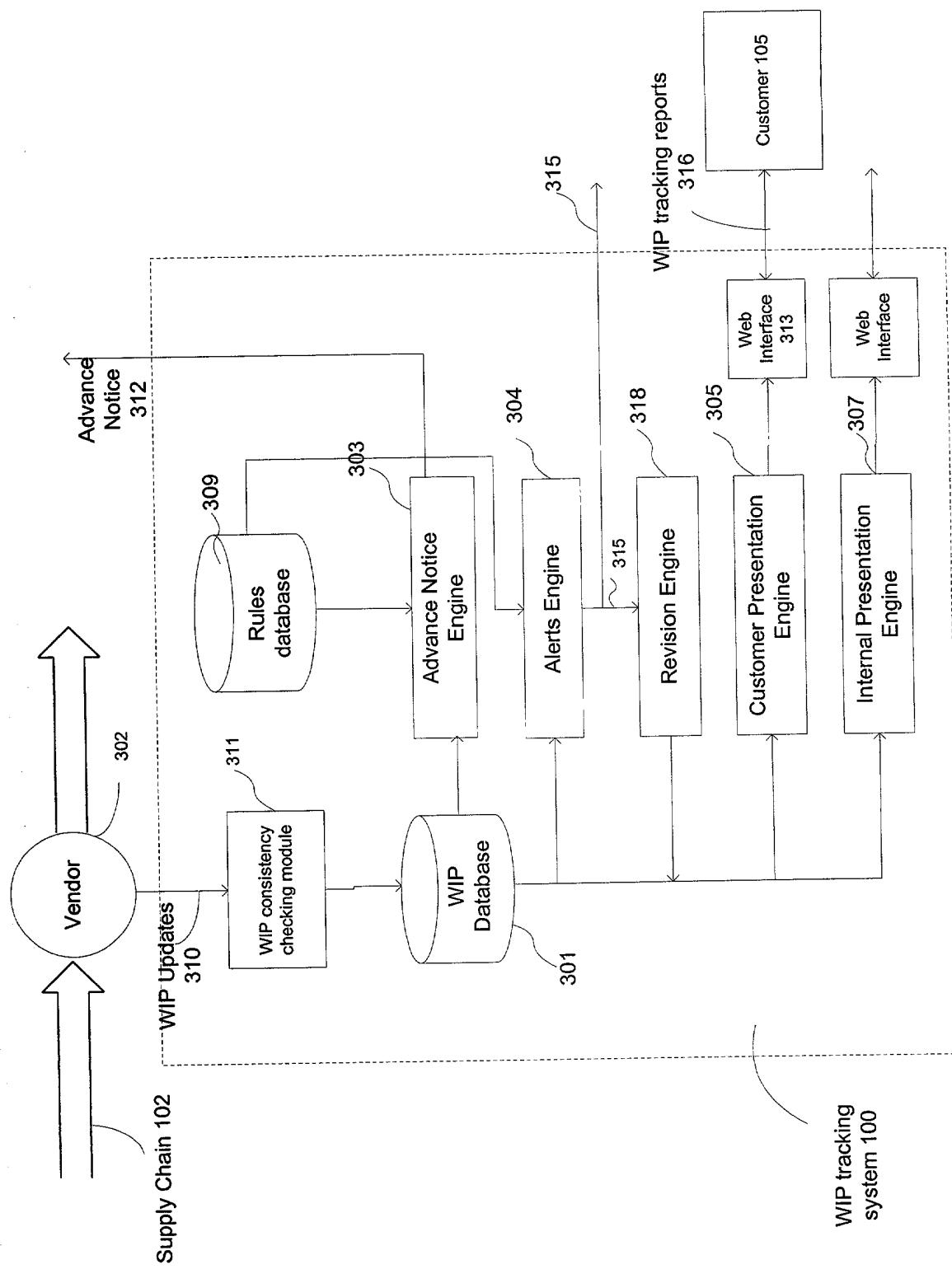


FIG. 3

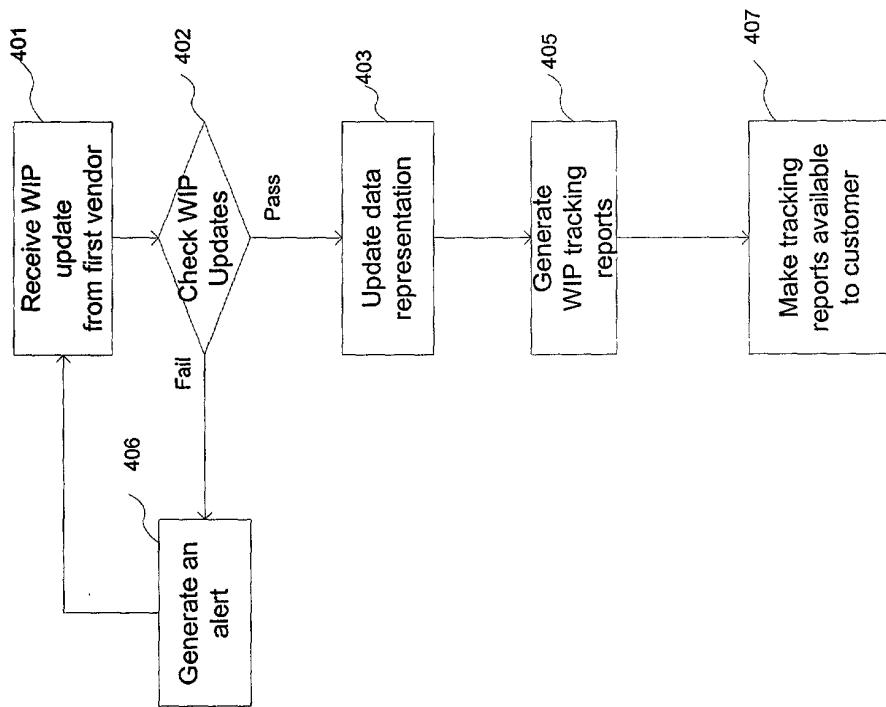
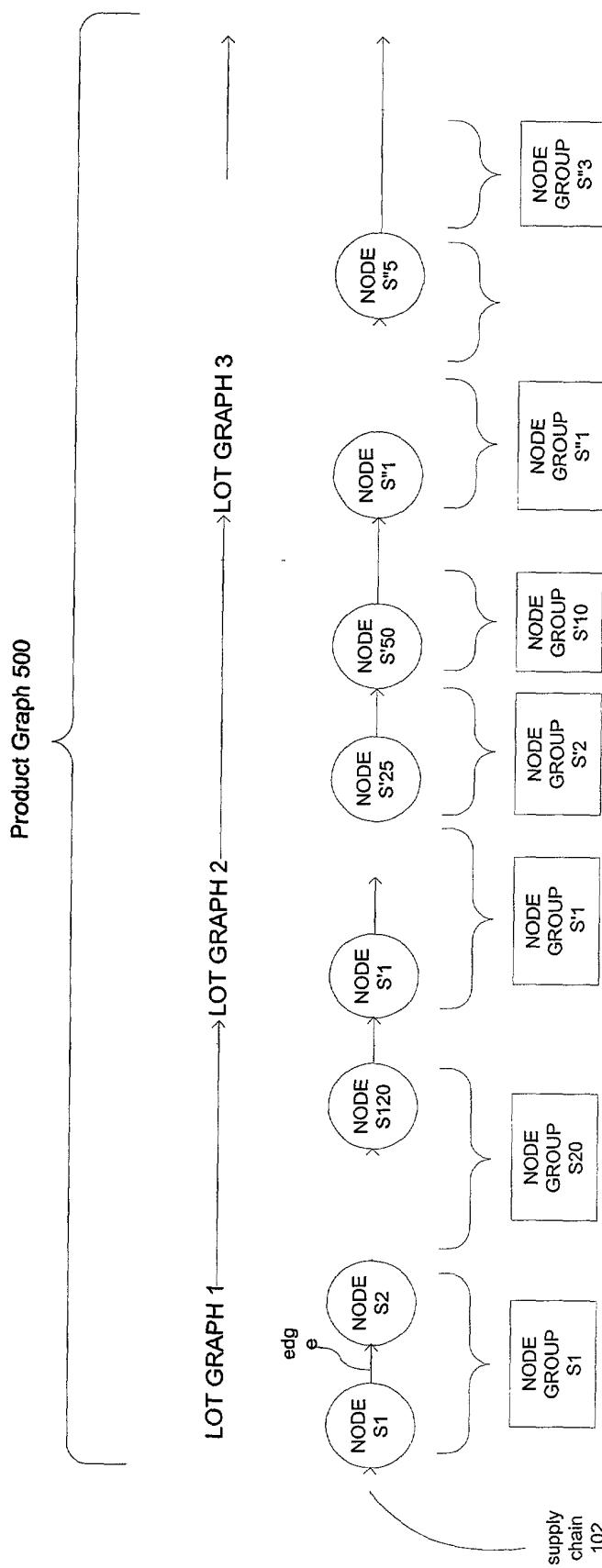


FIG. 4



5
FIG.

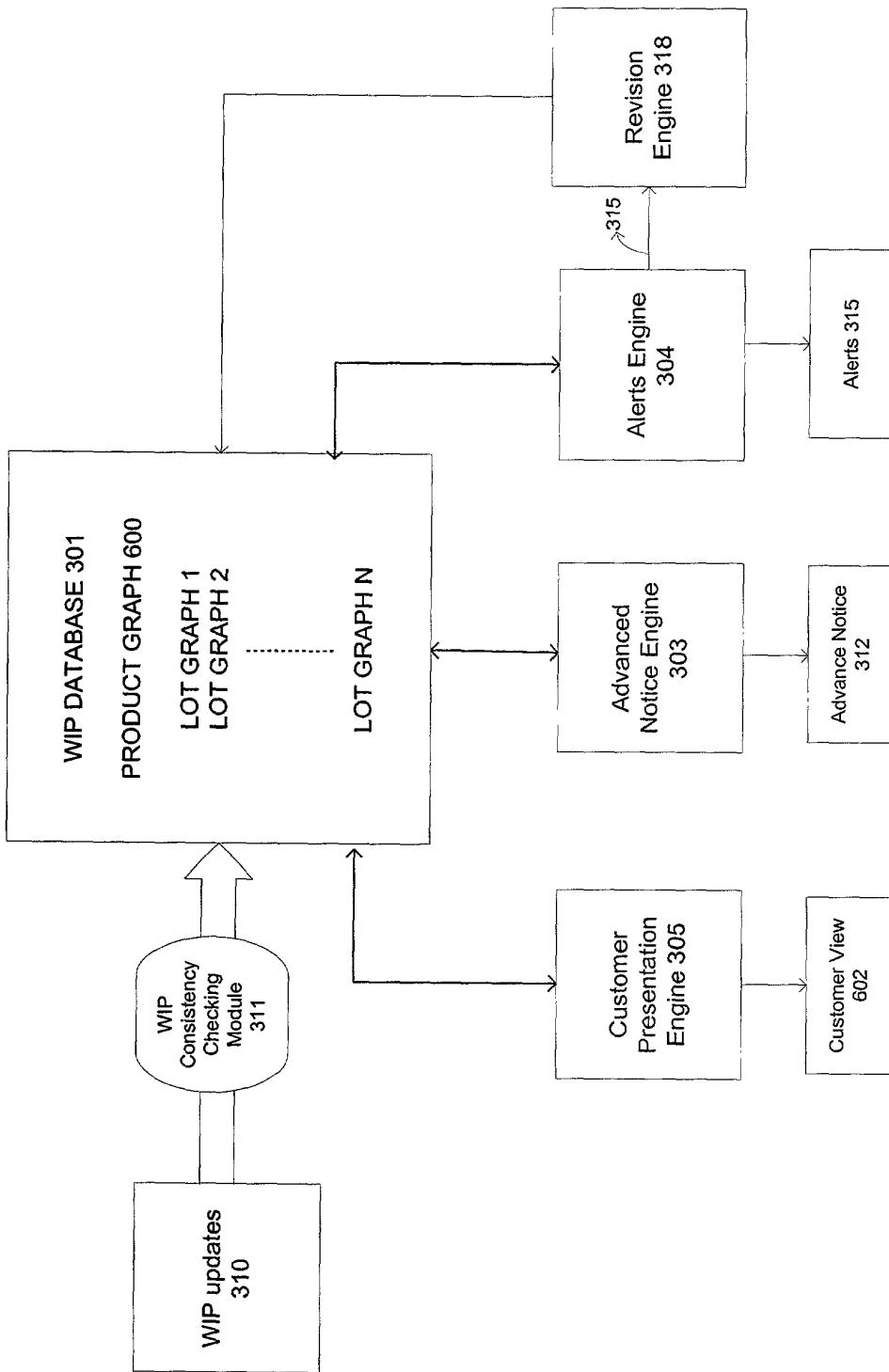


FIG. 6

PRODUCT GRAPH 600			
LOT GRAPH 1			
Node 10			
	Original	Actual	intRevised
Start Date	12/31	---	12/31
Duration	1	---	1
QTY	---	---	---

Node 11			
	Original	Actual	intRevised
Start Date	1/1	---	1/1
Duration	1	---	1
QTY	---	---	---

Process Flow 709 for Lot ID 702		
Step	Expected Duration	Conversion Factor
10	1	200
11	1	200

FIG. 7A

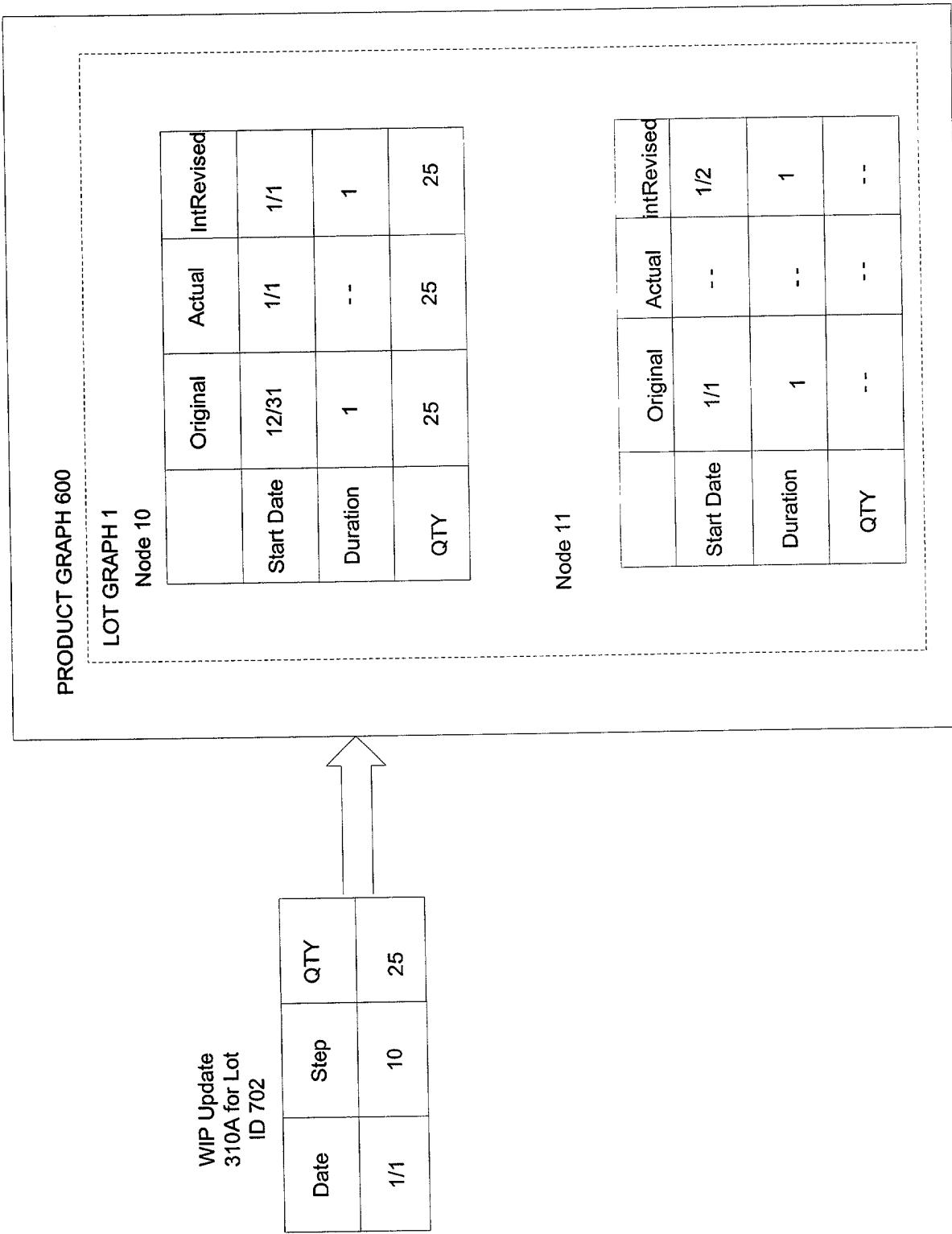


FIG. 7B

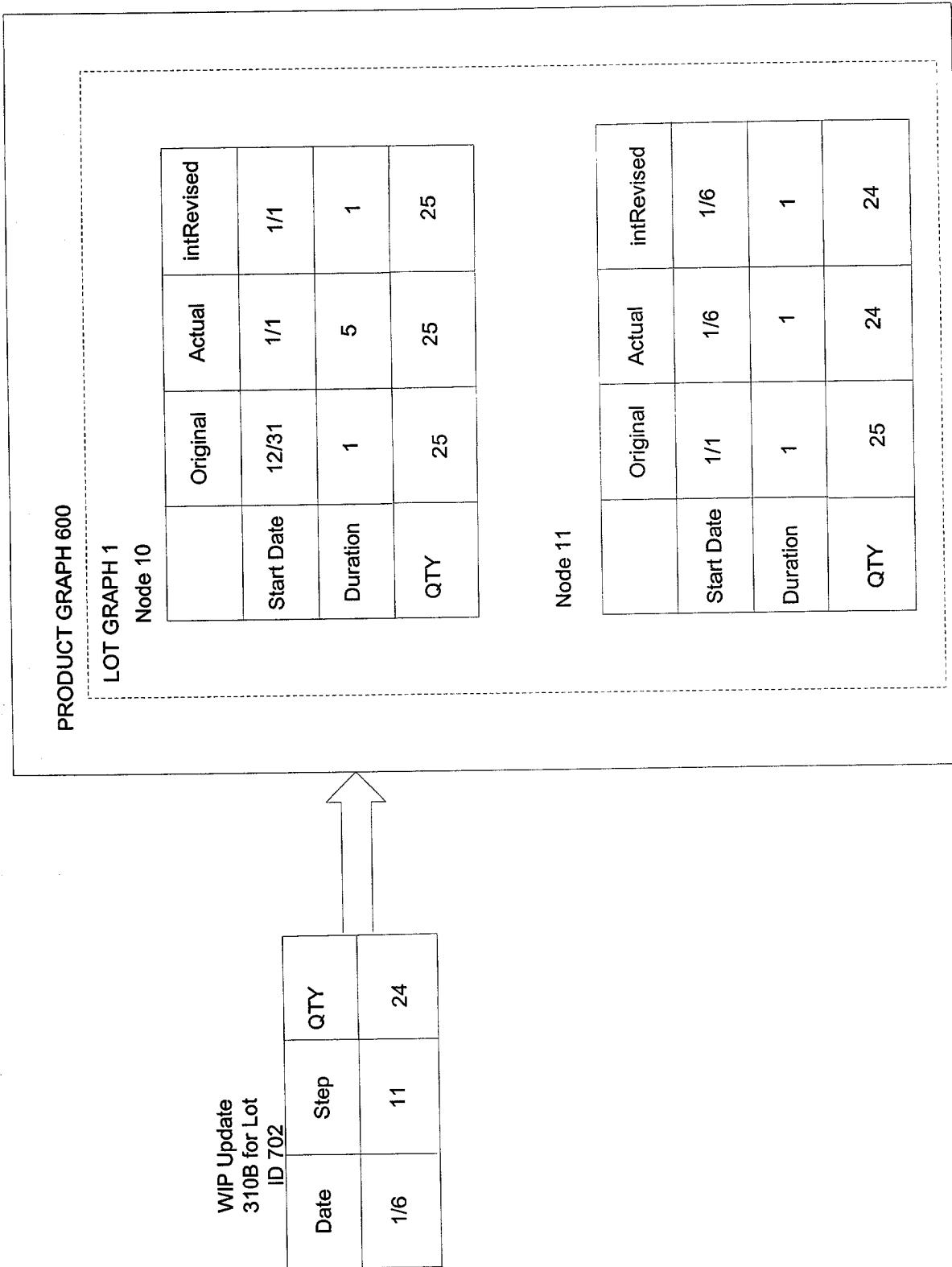


FIG. 7C

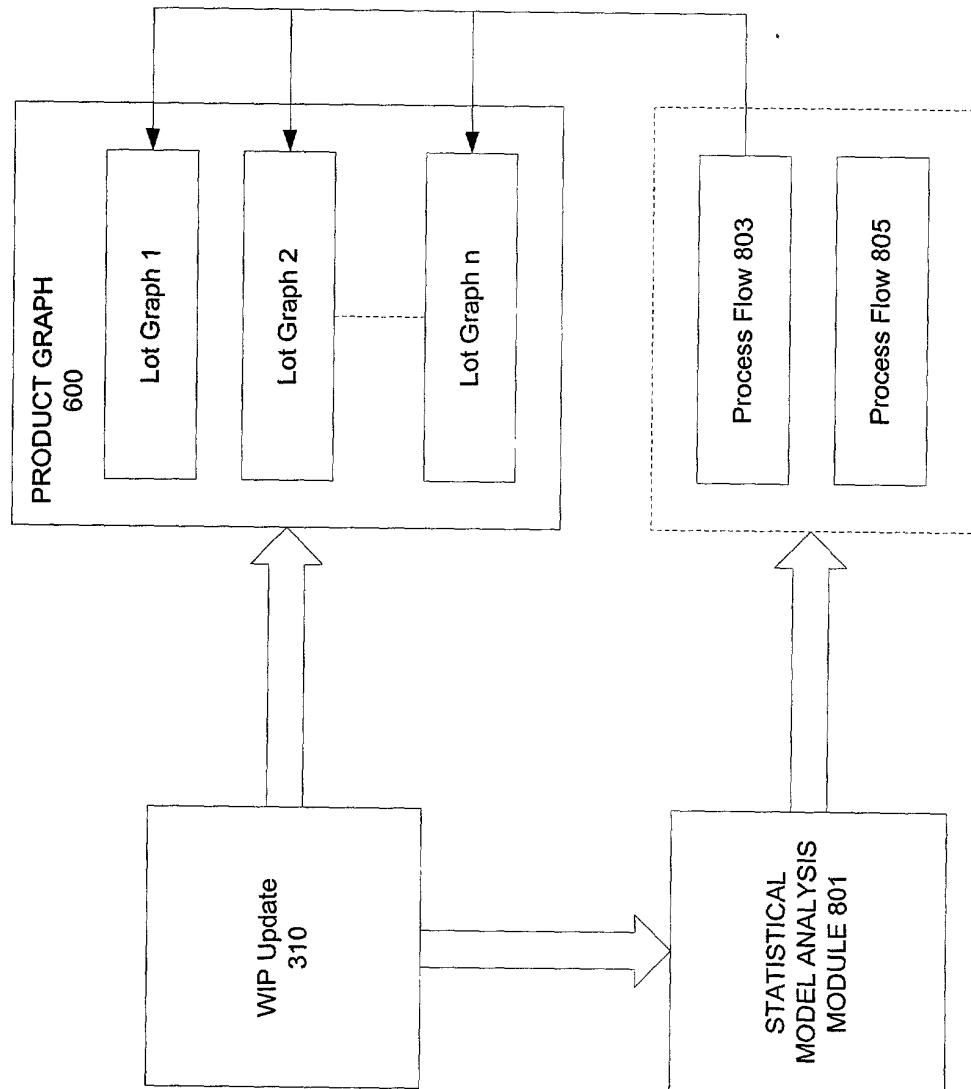


FIG. 8

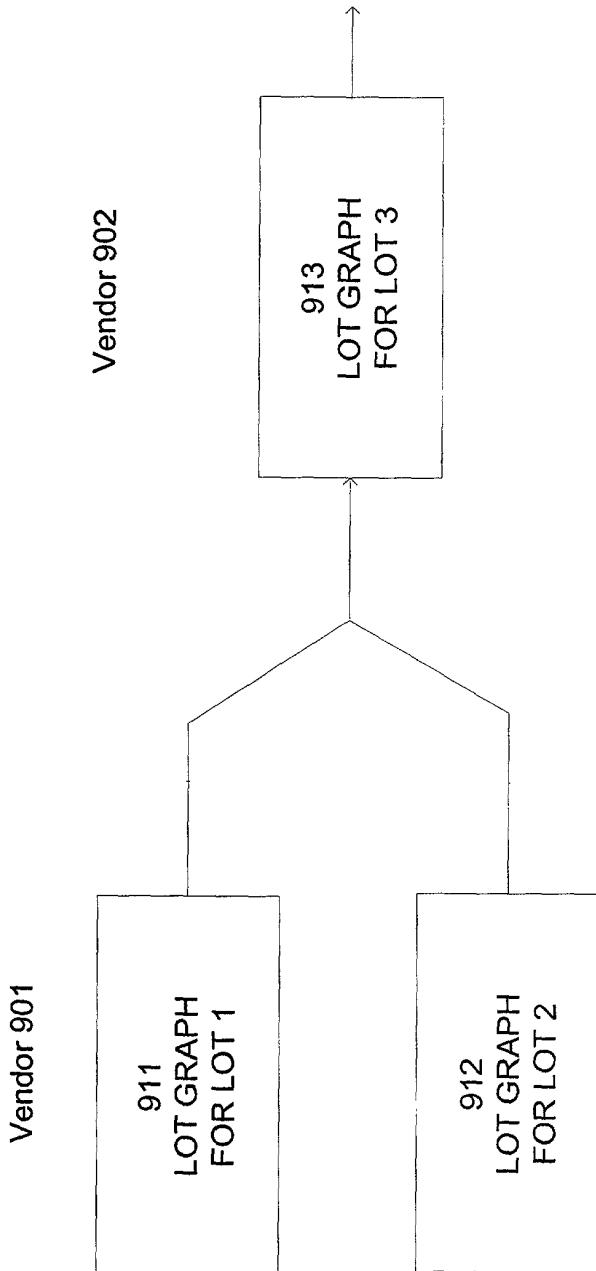


FIG. 9

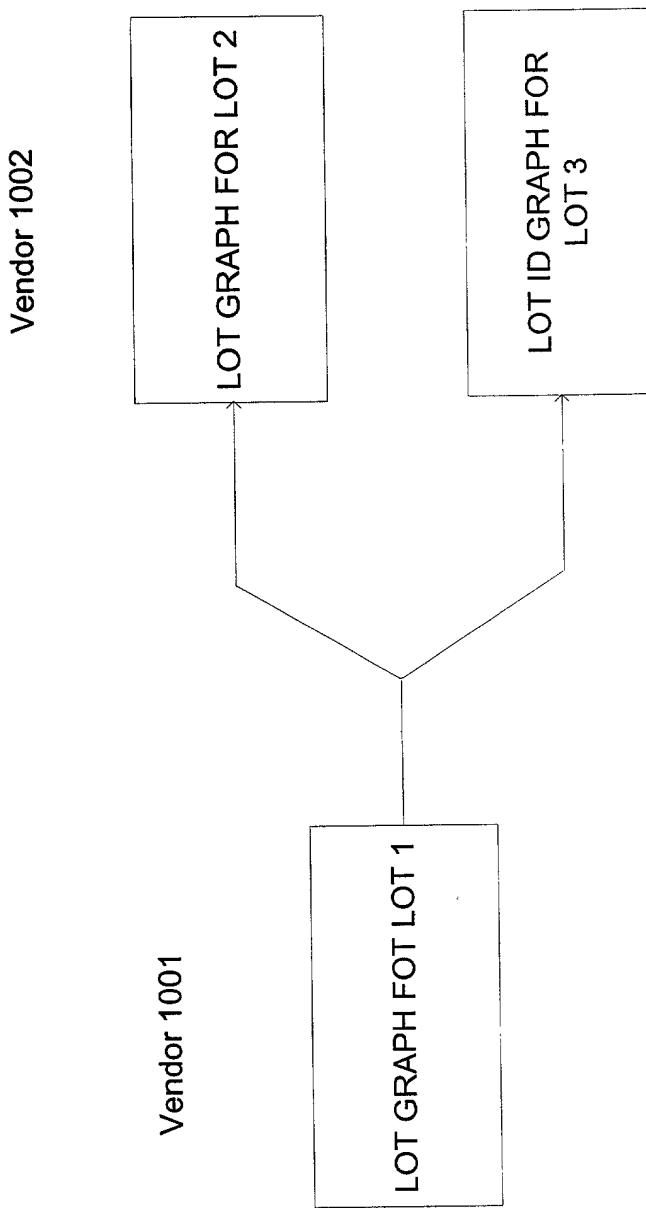


FIG. 10

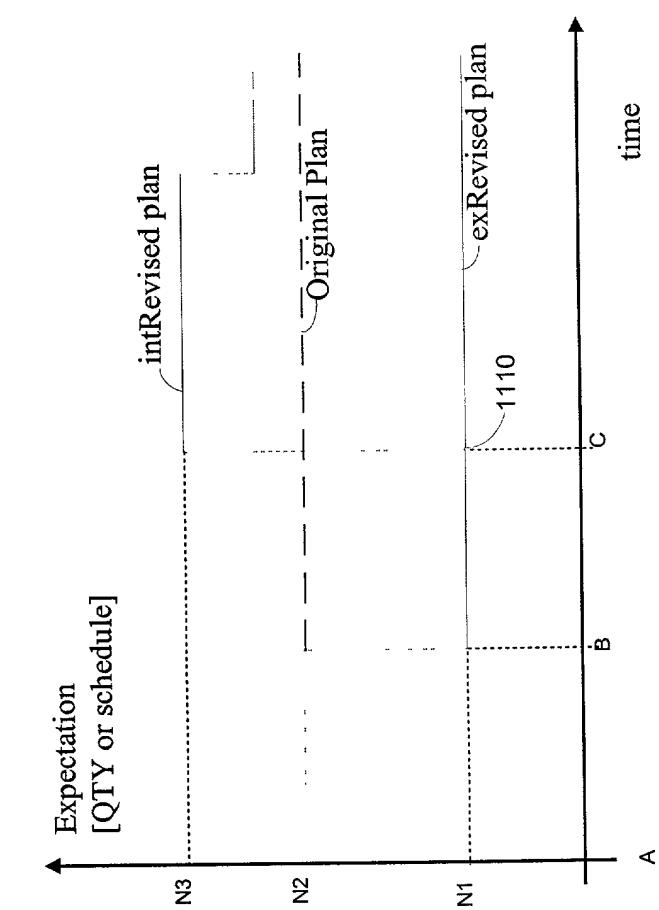


FIG. 11

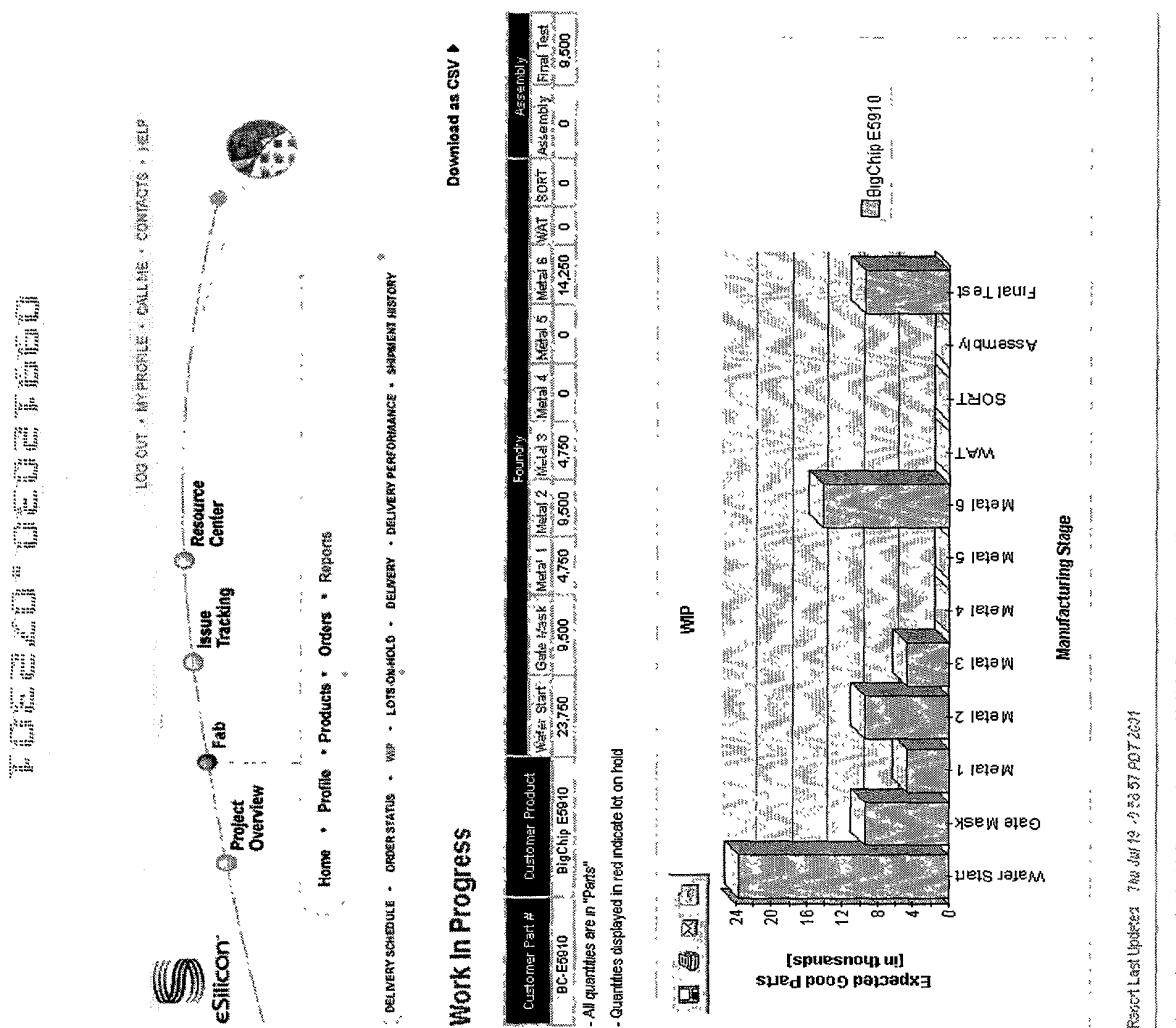


FIG. 12A

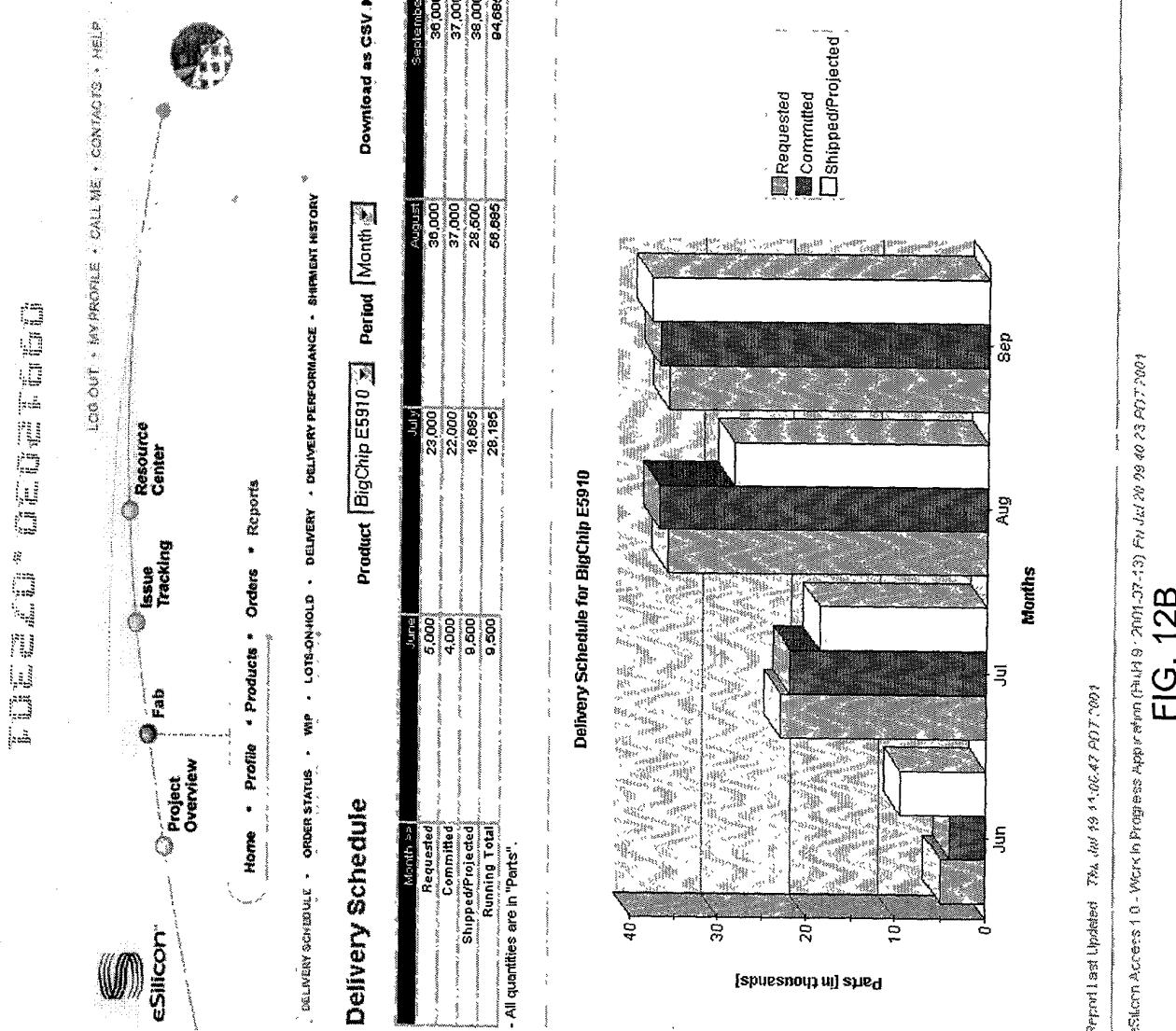


FIG. 12B

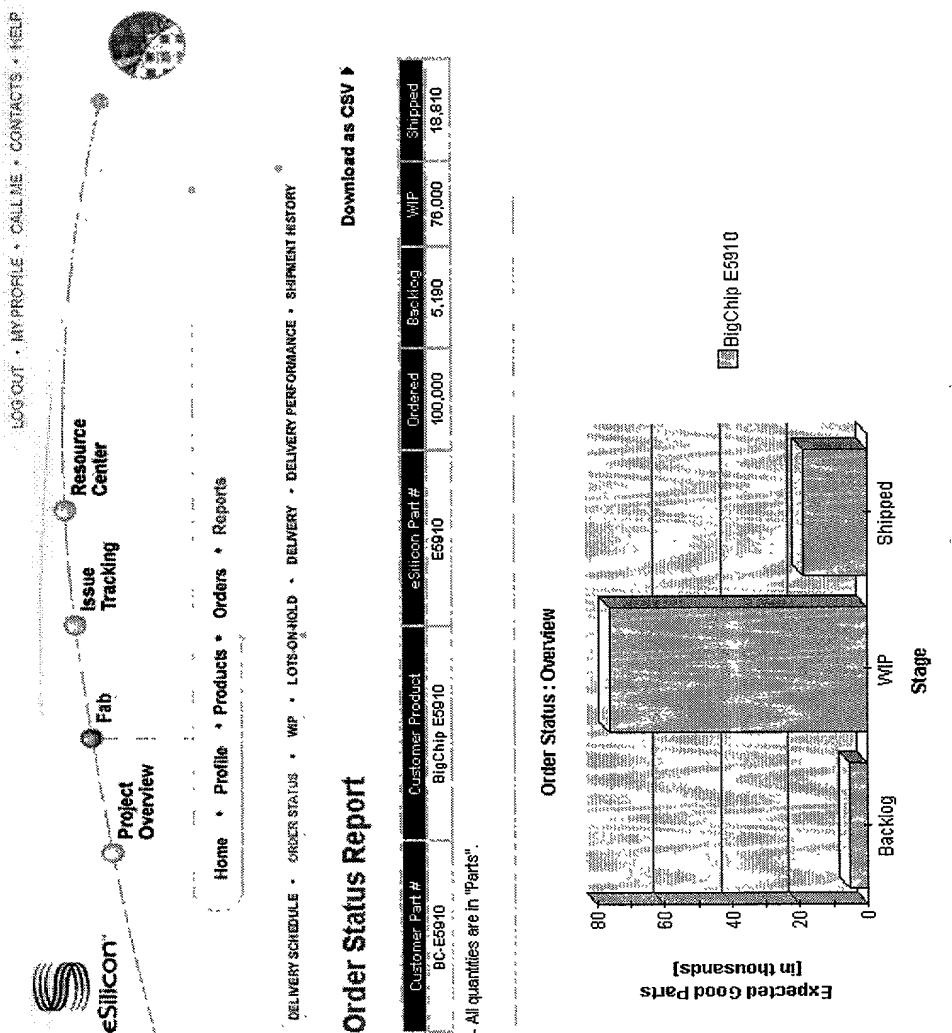


FIG. 12C